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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/466,964	12/20/1999	GAD S. SHEAFFER	2207/7533	1789

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EXAMINER	
NGUYEN, MIKE	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 04/22/2004

15

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/466,964	Applicant(s) SHEAFFER, GAD S.	
	Examiner Mike Nguyen	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-14, 21-22 and 28-30* is/are allowed.

6)☒ Claim(s) *15-20 and 23-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notices & Remarks

1. Applicant's amendment 10/29/2004 in response to Examiner's Office Action has been reviewed.

2. Claims 1-30 are pending for the examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 15-20 and 23-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Bitner Haim (U.S. Pat. No. 5,210,829).

As to claim 15, Bitner teaches an apparatus to control the loading of a memory buffer, comprising:

a memory buffer (see figure 1 element 34); and

a memory controller to receive an advance indication of a memory service interruption, coupled to said memory buffer (see fig. 1 element 32 col. 6 line 59 to col. 7 line 2 and fig. 4 WRITE CYCLE # 9-10 col. 14 lines 29-61 wherein at the WRITE CYCLE # 9 the memory buffer 34 receives an advance indication that indicates no host stall occurred), including

a watermark register (see figure 4 WRITE CYCLE # 8-12 and column 14 lines 29-61 and column 15 lines 1-14 wherein the watermark is adjustable to maximize the availability of

the buffer to receive data from the host computer 20 therefore it is obviously the controller having a watermark register);

a first register, coupled to said watermark register, to store a first watermark value (see figure 4 WRITE CYCLE # 9 and column 14 lines 29-61 and column 15 lines 1-14 wherein assumed that the memory buffer 34 has a first watermark value at the WRITE CYCLE # 9; therefore, it is obviously the controller has a first register); and

a second register, coupled to said watermark register, to store a second watermark value (see figure 4 WRITE CYCLE # 11 and column 14 lines 29-61 and column 15 lines 1-14 wherein the watermark is advanced to a second watermark value 430 Kb; therefore, it is obviously the controller has a second register).

As to claim 16, Bitner teaches the apparatus of claim 15, wherein the memory controller includes:

a below-watermark burst size register (see figure 4 WRITE CYCLE #9 and column 14 lines 29-61);

a third register, coupled to said below-watermark burst size register, to store a first below-watermark burst size value (see figure 4 WRITE CYCLE # 12 and column 15 lines 1-14); and

a fourth register, coupled to said below-watermark burst size register, to store a second below-watermark burst size value (see column 15 lines 1-14).

As to claims 17 and 20, Bitner teaches the memory controller is to:

read the second watermark value from said second register based at least in part on the received advance indication of a memory service interruption (see figure 4 WRITE CYCLE # 9-10 and column 14 lines 29-61); and

store the second watermark value in said watermark register (see figure 4 WRITE CYCLE # 9-10 and column 14 lines 29-61).

As to claim 18, Bitner teaches the apparatus of claim 16, wherein the memory controller is to:

read the second watermark value from said second register based at least in part on the received advance indication of a memory service interruption (see figure 4 WRITE CYCLE # 9-10 and column 14 lines 29-61); and

store the second watermark value in said watermark register (see figure 4 WRITE CYCLE # 9-10 and column 14 lines 29-61)

read the second below-watermark burst size value from said fourth register based at least in part on the received advanced indication of a memory service interruption (see figure 4 and column 14 lines 29-31); and

store the second below-watermark burst size value in said below-watermark burst size register (see figure 4 and column 14 lines 29-31).

As to claim 19, Bitner teaches a system to process video signals, the system comprising:

a processor (see fig. 1);

a memory, coupled to said processor (see fig. 1).

a memory buffer (see fig. 1 element 34); and

a memory controller to receive an advance indication of a memory service interruption, coupled to said memory buffer (see fig. 1 element 32 col. 6 line 59 to col. 7 line 2 and fig. 4 WRITE CYCLE # 9-10 col. 14 lines 29-61 wherein at the WRITE CYCLE # 9 the memory buffer 34 receives an advance indication that indicates no host stall occurred), including

a watermark register (see figure 4 WRITE CYCLE # 8-12 and column 14 lines 29-61 and column 15 lines 1-14 wherein the watermark is adjustable to maximize the availability of the buffer to receive data from the host computer 20 therefore it is obviously the controller having a watermark register);

a first register, coupled to said watermark register, to store a first watermark value (see figure 4 WRITE CYCLE # 9 and column 14 lines 29-61 and column 15 lines 1-14 wherein assumed that the memory buffer 34 has a first watermark value at the WRITE CYCLE # 9; therefore, it is obviously the controller has a first register); and

a second register, coupled to said watermark register, to store a second watermark value (see figure 4 WRITE CYCLE # 11 and column 14 lines 29-61 and column 15 lines 1-14 wherein the watermark is advanced to a second watermark value 430 Kb; therefore, it is obviously the controller has a second register).

As to claim 23, Bitner teaches an apparatus comprising:

a memory buffer (see fig. 1 element 34); and

a memory controller coupled to said memory controller, said memory controller to

operate in a first mode maintaining a first level of buffering in said memory buffer and to switch to a second mode maintaining a second level of buffering that is higher than the first level of buffering in response to an advance indication of a memory service interruption (see fig. 1 element 32 col. 6 line 59 to col. 7 line 2 and fig. 4 WRITE CYCLE # 9-10 col. 14 lines 29-61 wherein at the WRITE CYCLE # 9 the memory buffer 34 receives an advance indication that indicates no host stall occurred).

As to claim 24, Bitner teaches the apparatus of claim 23 wherein said memory service interruption is a DRAM refresh operation (see figure 1 and column 6 lines 59-67).

As to claim 25, Bitner teaches the apparatus of claim 23 wherein said memory service interruption is a memory maintenance operation (see figure 1 wherein the buffer 3 is used temporarily to store data sent by host computer 20 so that the watermark adjusts up and down based on the maintenance operation of the host computer 20).

As to claim 26, Bitner teaches the apparatus of claim 23 wherein said first mode has an associated first burst size and said second mode has an associated second burst size (see figure 4 column 14 lines 29-61 and column 15 lines 1-14).

As to claim 27, Bitner teaches the apparatus of claim 3 wherein said memory buffer is a video buffer to buffer a video stream retrieved from memory (see column 25 lines 14-19).

Allowable Subject Matter

5. Claims 1-14, 21-22 and 28-30 are allowed.

Response to Arguments

6. In response to the applicant's arguments that Bitner fails to teach "receiving advance indication of a memory service interruption by a memory controller". Examiner disagrees, in see fig. 4 WRITE CYCLE # 9-10 and col. 14 lines 29-61 clearly indicates that the watermark is modified from the first watermark value 420 Kb to the second watermark value 430 Kb based on receive advance indication of the host (no host stall occurred). Therefore buffering level is adjusted whenever the buffer receives an advance indication of the host.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 5,542,076 (Benson et al.)

U.S. Pat. No. 5,367,689 (Mayer et al.)

U.S. Pat. No. 5,179,707 (Piepho)

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is 703 305-5040. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Nguyen
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04/19/2004

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